

ABSTRACT

The present invention achieves the enhancement of a manufacturing yield factor and the reduction of manufacturing cost in a manufacturing method of a semiconductor device having a hetero junction bipolar transistor (HBT), a Schottky diode and a resistance element. The present invention is directed to the manufacturing method of a semiconductor device in which respective semiconductor layers which become a sub collector layer, a collector layer, a base layer, a wide gap emitter layer and an emitter layer are sequentially formed over one surface of a semiconductor substrate and, thereafter, respective semiconductor layers are processed to form the hetero junction bipolar transistor, the Schottky diode and the resistance element in a monolithic manner. An emitter electrode of the hetero junction bipolar transistor, a Schottky electrode of the Schottky diode and a resistance film of the resistance element are simultaneously formed using a same material (for example, WSiN). Accordingly, the man-hours can be reduced and the manufacturing cost of the semiconductor device can be reduced.